IN THE CLAIMS

1. (Original) A traffic management processor for processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit for calculating a departure time for each packet received;

a content addressable memory (CAM) device coupled to the DTC circuit and having a plurality of rows, each row including a first portion for storing the departure time for a corresponding packet and including a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow; and

compare logic coupled to the CAM device and configured to determine which of the departure times stored in the CAM device is the earliest.

2. (Original) The traffic management processor of Claim 1, wherein the packets of the CBR traffic flow and packets of the UBR traffic flow are queued in the same queuing mechanism.

3. (Original) The traffic management processor of Claim 1, wherein an asserted CBR bit indicates the departure time corresponds to a packet of the CBR traffic flow, and a de-asserted CBR bit indicates the departure time corresponds to a packet of the UBR traffic flow.

4. (Original) The traffic management processor of Claim 3, wherein only the departure times for packets having a de-asserted CBR bit participate in determining which departure time is the earliest.

5. (Original) The traffic management processor of Claim 1, wherein the departure times comprise counter values generated by a counter circuit in response to state transitions of a clock signal.

6. (Original) The traffic management processor of Claim 1, wherein the departure times can be stored in the CAM device in any order, regardless of priority.

7. (Original) The traffic management processor of Claim 1, further comprising a priority encoder coupled to the compare logic.

8. (Original) The traffic management processor of Claim 1, further comprising:

a match line coupled to each row of the CAM device;

a word line coupled to each row of the CAM device; and

means for selectively driving each word line in response to a match condition indicated on the corresponding match line.

9. (Original) The traffic management processor of Claim 1, wherein the compare logic is configured to compare the departure times provided by the CAM device with each other to determine which departure time is the earliest.

10. (Original) The traffic management processor of Claim 9, wherein the CAM device selectively provides the departure times to the compare logic in response to the CBR bits.

11. (Original) The traffic management processor of Claim 10, wherein the departure times corresponding to packets of the CBR traffic flow are not provided to the compare logic.

12. (Original) The traffic management processor of Claim 1, wherein the CAM device further includes an input to receive a current time value.

13. (Original) The traffic management processor of Claim 12, wherein the CAM device is configured to compare the current time value to only those departure

times having an asserted CBR bit.

14. (Original) The traffic management processor of Claim 13, wherein the CAM device is configured to selectively de-assert the CBR bits in response to match conditions in the CAM device.

15. (Original) The traffic management processor of Claim 14, wherein de-assertion of the CBR bit enables the corresponding departure time to participate in determining which departure time is the earliest.

16. (Currently Amended) A traffic management processor for processing a plurality of packets each having a control bit indicating whether the packet belongs to a traffic flow having an unspecified bit rate (UBR) or belongs to a traffic flow having a constant bit rate (CBR), comprising:

means for generating a departure time for each packet in response to the control bit contained within the packet;

means for queuing the CBR packets and the UBR packets together in the same queue according to their departure times; and

means for selecting the CBR packets and the UBR packets for transmission according to their departure times.

17. (Original) The traffic management processor of Claim 16, wherein the means for generating comprises:

a departure time calculator configured to calculate the departure times for CBR packets using a first expression and to calculate the departure times for UBR packets using a second expression.

18. (Original) The traffic management processor of Claim 16, wherein the means for queuing comprises:

a content addressable memory (CAM) device having a plurality of rows, each row including a first portion for storing the departure time for a corresponding packet and including a second portion for storing the control bit.

19. (Original) The traffic management processor of Claim 18, wherein the CAM device includes an input to receive a current time value and is configured to compare the current time value with the departure times of the CBR packets.

20. (Original) The traffic management processor of Claim 18, wherein the means for selecting comprises:

compare logic coupled to the CAM device and configured to determine which of the departure times for the UBR packets and for the re-classified CBR packets is the earliest.

21. (Original) The traffic management processor of Claim 20, wherein the compare logic compares the departure times with each other to determine which of the departure times is the earliest.

22. (Original) A traffic management processor for simultaneously processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit configured to calculate a departure time for each UBR packet and configured to calculate a departure time window for each CBR packet;

a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together; and

compare logic coupled to the queuing mechanism and configured to select the packets for departure.

23. (Original) The traffic management processor of Claim 22, wherein the queuing mechanism is configured to always enable the UBR packets for departure and

configured to selectively enable the CBR packets for departure.

24. (Original) The traffic management processor of Claim 23, wherein the queuing mechanism enables each CBR packet for departure when the CBR packet's departure time window comprises a current time value.

25. (Original) The traffic management processor of Claim 24, wherein the queuing mechanism comprises a content addressable memory (CAM) device.

26. (Original) The traffic management processor of Claim 25, wherein the CAM device comprises:

a plurality of rows, each row having a first portion for storing the departure time for a corresponding packet and having a second portion for storing a control bit indicating whether the corresponding packet is part of the UBR traffic flow or is part of the CBR traffic flow; and

an input to receive the current time value.

27. (Original) The traffic management processor of Claim 22, wherein the compare logic compares the departure times with each other to determine which of the departure times is the earliest.

28. (Original) A method of processing a first traffic flow having an unspecified bit rate (UBR) and a second traffic flow having a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit;

asserting the CBR bit for each packet that belongs to the CBR traffic flow;

de-asserting the CBR bit for each packet that belongs to the UBR traffic flow;

determining which of the departure times that have a de-asserted CBR bit is the earliest; and

transmitting the packet corresponding to the earliest departure time.

29. (Original) The method of Claim 28, wherein the departure times having de-asserted CBR bits are compared with each other to determine which departure time is the earliest.

30. (Original) The method of Claim 28, wherein the table comprises a content addressable memory.

31. (Original) The method of Claim 28, further comprising:

comparing a current time value with the departure times having asserted CBR bits; and

de-asserting the CBR bit corresponding to the departure time that matches the current time value.

32. (Original) The method of Claim 31, wherein de-asserting the CBR bit enables the corresponding departure time to participate in determining which departure time is the earliest.

33. (Original) A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for the UBR packets and for the CBR packets in a content addressable memory (CAM) device;

comparing the departure times for the UBR packets with each other to determine which departure time is the earliest; and

transmitting the packet corresponding to the earliest departure time.

34. (Original) The method of Claim 33, further comprising:

comparing a current time value with the departure times for the CBR packets.

35. (Original) A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each UBR packet;

calculating a departure time window for each CBR packet;

queuing the CBR packets and the UBR packets together in the same queuing mechanism; and

selecting the packets for departure according to which packet has the earliest departure time.

36. (Original) The method of Claim 35, further comprising:

comparing a current time value with the departure time windows for the CBR packets; and

selectively enabling the CBR packets to participate in determining which packet has the earliest departure time in response to the comparing.